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Method Of Forming Non-Volatile Resistance Variable Devices

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INVENTORS

Kristy A. Campbell
Terry L. Gilton
John T. Moore
Jiutao Li

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Method Of Forming Non-Volatile Resistance Variable Devices

TECHNICAL FIELD

This invention relates to methods of forming non-volatile resistance variable devices, for example to methods of forming a programmable memory cell of memory circuitry.

BACKGROUND OF THE INVENTION

Semiconductor fabrication continues to strive to make individual electronic components smaller and smaller, resulting in ever denser integrated circuitry. One type of integrated circuitry comprises memory circuitry where information is stored in the form of binary data. The circuitry can be fabricated such that the data is volatile or non-volatile. Volatile storing memory devices result in loss of data when power is interrupted. Non-volatile memory circuitry retains the stored data even when power is interrupted.

This invention was principally motivated in making improvements to the design and operation of memory circuitry disclosed in the Kozicki et al. U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, which ultimately resulted from U.S. Patent Application Serial No. 08/652,706, filed on May 30, 1996, disclosing what is referred to as a programmable metallization cell. Such a cell includes opposing electrodes having an insulating dielectric material received therebetween. Received within the dielectric material is a fast ion

conductor material. The resistance of such material can be changed between highly insulative and highly conductive states. In its normal high resistive state, to perform a write operation, a voltage potential is applied to a certain one of the electrodes, with the other of the electrode being held at zero voltage or ground. The electrode having the voltage applied thereto functions as an anode, while the electrode held at zero or ground functions as a cathode. The nature of the fast ion conductor material is such that it undergoes a structural change at a certain applied voltage. With such voltage applied, a conductive dendrite or filament extends between the electrodes, effectively interconnecting the top and bottom electrodes to electrically short them together.

Once this occurs, dendrite growth stops, and is retained when the voltage potentials are removed. Such can effectively result in the resistance of the mass of fast ion conductor material between electrodes dropping by a factor of 1,000. Such material can be returned to its highly resistive state by reversing the voltage potential between the anode and cathode, whereby the filament disappears. Again, the highly resistive state is maintained once the reverse voltage potentials are removed. Accordingly, such a device can, for example, function as a programmable memory cell of memory circuitry.

The preferred resistance variable material received between the electrodes typically and preferably comprises a chalcogenide material having metal ions diffused therein. A specific example is germanium selenide having silver ions diffused therein. The present method of providing the silver ions within the germanium selenide material is to initially chemical vapor deposit the germanium

selenide glass without any silver being received therein. A thin layer of silver is thereafter deposited upon the glass, for example by sputtering, physical vapor deposition or other technique. An exemplary thickness is 200 Angstroms or less. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 500 nanometers. The thin nature of the deposited silver enables such energy to pass through the silver to the silver/glass interface effective to break a chalcogenide bond of the chalcogenide material. This may form Ag_2Se, which effectively dopes the glass with silver.

Saturation of silver in germanium selenide is apparently at a maximum of about 34 atomic percent or less depending on the germanium selenide stoichiometry. Yet, preferred existing technology for cell fabrication constitutes a concentration which is less than the maximum; in the case of 34 atomic percent maximum, an example concentration would be about 27 atomic percent.

After the chalcogenide comprising material is provided with silver to a desired concentration, the top electrode material (typically silver) is next deposited. But, as the silver doping/diffusion into the chalcogenide material approaches the maximum or saturation, some Ag_2Se was discovered to form at the surface and remain there as opposed to diffusing into the glass. Further, the surface Ag_2Se was typically in the form of semicircular nodules or bumps anywhere from 50 Angstroms to 20 microns across. Unfortunately when the typical silver electrode material is subsequently deposited, such tends to mound on top of these previous bumps. This can create voids to the doped germanium glass through the top electrode material, whereby the silver doped

germanium selenide glass is partially exposed. Unfortunately, some of the photodeveloper solutions typically used for patterning the top electrode (i.e. tetramethyl ammonium hydroxide) will etch the glass that is exposed.

It would be desirable to overcome or at least reduce this problem. While the invention was principally motivated in overcoming this problem, it is in no way so limited. The artisan will appreciate applicability of the invention in other aspects unrelated to the problem, with the invention only being limited by the accompanying claims as literally worded and as appropriately interpreted in accordance with the doctrine of equivalents.

SUMMARY

The invention includes methods of forming a programmable memory cell of memory circuitry and non-volatile resistance variable devices. In one implementation, a method of forming a non-volatile resistance variable device includes forming a first conductive electrode material on a substrate. A metal doped chalcogenide comprising material is formed over the first conductive electrode material. The chalcogenide comprising material comprises the metal and A_xB_y, where "B" is selected from the group consisting of S, Se and Te and mixtures thereof; and where "A" comprises at least one element which is selected from Group 13, Group 14, Group 15, or Group 17 of the periodic table. A passivating material is formed over the metal doped chalcogenide comprising material. A second conductive electrode material is formed over the passivating material. The second conductive electrode material is formed into an electrode of the device.

In one implementation, a method of forming a non-volatile resistance variable device includes forming a first conductive electrode material on a substrate. A metal doped chalcogenide comprising material is formed over the first conductive electrode material. The chalcogenide comprising material comprises the metal and A_xB_y, where "B" is selected from the group consisting of S, Se and Te and mixtures thereof, and where "A" comprises at least one element which is selected from Group 13, Group 14, Group 15, or Group 17 of the periodic table. The metal doped chalcogenide electrode material has an outer surface. In one aspect, the outer surface is exposed to an HNO_3

solution. In one aspect, the outer surface is oxidized effective to form a layer comprising at least one of an oxide of "A" or an oxide of "B". After the oxidizing, a second conductive electrode material is deposited over the layer, and a second conductive electrode material of the device is ultimately formed therefrom.

Other implementations and aspects are contemplated and disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

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Fig. 4 is a view of the Fig. 1 wafer fragment at an alternate processing step to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment 10 is shown in but one preferred embodiment of a method of forming a non-volatile resistance variable device. By way of example only, example such devices include programmable metallization cells and programmable optical elements of the patents referred to above, further by way of example only, including programmable capacitance elements, programmable resistance elements, programmable antifuses of integrated circuitry and programmable memory cells of memory circuitry. The above patents are herein incorporated by reference. The invention contemplates the fabrication techniques and structure of any existing non-volatile resistance variable device, as well as yet-to-be developed such devices. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural unless

otherwise indicated. Further, it will be appreciated by the artisan that "resistance variable device" includes devices wherein a property or properties in addition to resistance is/are also varied. For example, and by way of example only, the device's capacitance and/or inductance might also be changed in addition to resistance.

Semiconductor wafer fragment 10 comprises a bulk monocrystalline semiconductive material 12, for example silicon, having an insulative dielectric layer 14, for example silicon dioxide, formed thereover. A first conductive electrode material 16 is formed over dielectric layer 14. By way of example only, preferred materials include any of those described in the incorporated Kozicki et al. patents referred to above in conjunction with the preferred type of device being fabricated. A dielectric layer 18 is formed over first electrode material 16. Silicon nitride is a preferred example.

An opening 20 is formed through layer 18 to conductive electrode layer 16. Such is filled with a chalcogenide comprising material 22 to a first thickness, which in this example is essentially defined by the thickness of layer 18. By way of example only, an exemplary first thickness range is from 100 Angstroms to 1000 Angstroms. The chalcogenide comprising material comprises A_xB_y, where "B" is selected from the group consisting of S, Se and Te and mixtures thereof, and where "A" comprises at least one element which is selected from Group 13 (B, Al, Ga, In, Tl), Group 14 (C, Si, Ge, Sn, Pb), Group 15 (N, P, As, Sb, Bi), or Group 17 (F, Cl, Br, I, At) of the periodic table. By way of example only, preferred elements for "A" are Ge and Si.

An example preferred method of forming material 22 over substrate 10 is by chemical vapor deposition to completely fill opening 20, followed by a planarization technique, for example chemical mechanical polishing. Material 22 is preferably formed to be amorphous and remains amorphous in the finished device.

A metal comprising layer 24 is formed to a second thickness over chalcogenide comprising material 22. An example and preferred material for layer 24 is elemental silver. By way of example only, example alternates include zinc and copper. In one preferred embodiment, the second thickness is less than the first thickness. In one preferred embodiment, layer 24 is predominately (majority) elemental silver, and can consist or consist essentially of elemental silver.

Referring to Fig. 2, metal 24 is irradiated effective to break a chalcogenide bond of the chalcogenide comprising material at an interface of metal 24 and chalcogenide comprising material 22, and diffuse at least some of metal 24 into chalcogenide comprising material 22. In Fig. 2, material 22 is designated with numeral 23 and peppered in the drawings to indicate metal ions being received therein. A preferred irradiating includes exposure to actinic radiation having a wavelength from about 164 - 904 nanometers, with radiation exposure at between 404 - 408 nanometers being a more specific example. A more specific example is a flood UV exposure tool operating at 4.5 milliwatts/cm^2 energy for 15 minutes in an oxygen-containing ambient at room temperature and pressure. A mechanism of incorporation might include Ag_2Se

formation at the chalcogenide surface/interface, and diffusion doping thereof into material 22.

All of material 24 received directly over chalcogenide comprising material 22 might be diffused to within such material as shown, or only some portion thereof might. The thickness of layer 24 is also chosen to be suitably thin to enable the impinging electromagnetic radiation to essentially transparently pass through material 24 to the interface of such material with chalcogenide comprising material 22. The exemplary preferred thickness is as described above in comparison with the thickness of chalcogenide comprising material 22, and is preferably less than or equal to 200 Angstroms. The apparent linear thickness of layer 24 as a percentage of the linear thickness of chalcogenide comprising material 22 effectively results in the same approximate metal incorporation in atomic percent within the chalcogenide comprising material. Chalcogenide comprising material 22/23 can be considered as having an outer surface 25. Such provides but one example of forming a metal doped chalcogenide comprising material. Any other method in the context of this invention is contemplated, whether existing at the time of this writing or yet-to-be-developed.

Referring to Fig. 3, and in but one aspect of the invention, a passivating material 27 is formed at least over the metal doped chalcogenide comprising material. Passivating material 27 might be formed to be continuous and completely covering at least over the chalcogenide comprising material as shown in Fig. 3, or might be formed not to be continuous and not to be completely

covering over the chalcogenide comprising material as shown in an alternate embodiment of Fig. 4. In Fig. 4, like numerals from the first embodiment are utilized with differences being indicated by the suffix "a". Regardless, in the context of this document, a "passivating material" comprises a material the presence of which improves degree of continuity and covering over the chalcogenide comprising material of a subsequently deposited second conductive electrode material than would otherwise occur under identical deposition conditions for the second conductive electrode material but for presence of the passivating material. In one preferred embodiment, and as shown, the passivating material is formed on (in contact with) chalcogenide comprising material 23. The passivating material might comprise some form of oxide, nitride or material(s) which do/does not include oxides or nitrides. In one implementation, the passivating material is dielectric in nature. Passivating material 27/27a preferably is of a thickness from 1 Angstrom to 100 Angstroms, and more preferably from 1 Angstrom to 50 Angstroms. In one preferred implementation, the passivating material comprises an outer portion of the metal doped chalcogenide comprising material which is at least in part characterized by a higher concentration of "A" than metal doped chalcogenide comprising material immediately inwardly thereadjacent.

In one aspect, the passivating material is formed by exposing the substrate or outer surface 25 to ambient room temperature and pressure for a period of time effective to form the passivating material. In one aspect, the period of time is for at least 48 hours prior to a subsequent electrode material

deposition. In one aspect, the period of time is for at least 60 hours. In one aspect, the period of time is for at least 72 hours. In one aspect, the period of time is for at least 96 hours. In one aspect, at least the outer surface of the substrate is shielded from ambient room light during the exposing. In reduction to practice examples, substrates were placed within wafer storage boxes within a clean room environment. Such boxes shielded the substrates from ambient clean room light, provided static discharge isolation, but otherwise exposed the substrates to the clean room ambient including clean room temperature (about 20°C) and pressure (atmospheric). Significant improvement in continuity and covering of a subsequently deposited silver electrode layer occurred after exposure to such an ambient for 48 hours and prior to such silver deposition. Even greater improvement was demonstrated after 96 hours.

In one aspect, the passivating material is formed by exposing the outer surface to an atmosphere having a temperature elevated from ambient room temperature for a period of time effective to form the passivating material. The period of time will be at least in part dependent upon the atmosphere and the temperature. In one implementation, the atmosphere comprises oxygen. In another implementation, the atmosphere is substantially void of oxygen. Oxygen presence is expected to reduce the period of time.

In one aspect, the passivating material can be formed by exposing the substrate or outer surface 25 to a plasma comprising at least one of oxygen or hydrogen prior to a subsequent electrode material deposition. In one exemplary implementation where the plasma comprises oxygen, the plasma is

derived from a gas comprising O_2. In one exemplary implementation where the plasma comprises hydrogen, the plasma is derived from a gas comprising H_2. A preferred plasma tool for processing is a cold wall single wafer plasma sputtering system. Exemplary cathode power during processing in such a system is from about 100W to 400W for an eight inch wafer. Chuck power is preferably low to minimize etch effects. Exemplary chuck power is from about 3W to 10W for an eight inch wafer. Exemplary pressure during processing is from about 3 mTorr to about 50 mTorr. Exposure time can vary from a few seconds to several minutes, or more.

In one aspect, the passivating material can be formed by exposing the substrate or outer surface 25 to an aqueous solution prior to a subsequent electrode material deposition. In one preferred implementation, the aqueous solution consists essentially of H_2O. Other aqueous solutions are of course contemplated. Exemplary solution and exposure conditions include a temperature range from about 15°C to about 100°C. A preferred exposure pressure is clean room ambient. Exposure time can vary from a few seconds to several minutes, or more.

The passivating material formation can occur by other means, whether existing or yet to be developed, are also of course contemplated.

In one aspect, metal doped chalcogenide electrode material 23/outer surface 25 is oxidized effective to form the passivating material to comprise at least one of an oxide of "A" or an oxide of "B", and independent of constituting a "passivating material" as defined herein. In one preferred embodiment, the

passivating material is substantially continuous, at least over chalcogenide comprising material 23. In one preferred embodiment, the passivating material is preferably no greater than 50 Angstroms thick, with a preferred range being from 8 Angstroms to 50 Angstroms, and a specific preferred example being 10 Angstroms thick. Further in one preferred embodiment, the passivating material is formed to be dielectric. Further in one preferred embodiment, the layer comprises an oxide of "A". In one preferred embodiment, the layer comprises and oxide of "B". In one preferred embodiment, the layer comprises at least one oxide of "A" and at least one oxide of "B". One preferred method of oxidizing includes exposure to HNO_3, for example exposure to a HNO_3 solution. By way of example only, a concentration range for such HNO_3 solution is to provide one volume part of a 49 percent-by-volume HNO_3 solution in from one additional volume part of water to 100 additional volume parts of water. Exemplary exposure conditions include ambient temperature and pressure, although higher or lower temperature and/or pressure conditions from ambient are also of course contemplated. By way of example only, an exposure time might be anywhere from one second to ten minutes.

Further by way of example only, alternate exemplary oxidizing includes exposure to a fluid consisting essentially of H_2O, exposure to H_2O_2, exposure to O_2, and/or exposure to O_3. Further by way of example only, such O_2 or other exposure might be by an elevated temperature anneal at from 50°C to 133° at ambient, subatmospheric or higher pressure, and for an exemplary time range of anywhere from a few seconds to five hours.

The invention contemplates exposure of the outer surface of a chalcogenide comprising material in the context of the claimed combination to a HNO_3 solution independent of the stated effect of passivating, oxidizing, formation of a layer, or any other utility stated or inferred herein.

Referring to Fig. 5, after the oxidizing and/or passivating, a second conductive electrode material 26 is deposited over chalcogenide comprising material 23 and over material 27. Preferably as shown, material 26 is formed on (in contact with) material 27. In the preferred embodiment, such second conductive electrode material is continuous and completely covers at least over chalcogenide comprising material 23. An example preferred thickness range for second electrode material layer 26 is from 140 Angstroms to 200 Angstroms. The first and second conductive electrode materials might be the same material(s), or different material(s). By way of example only, preferred top and bottom electrode materials include silver, tungsten, platinum, nickel, carbon, chromium, molybdenum, aluminum, magnesium, copper, cobalt, palladium, vanadium, titanium, alloys thereof and compounds including one or more of these elements. In accordance with a preferred programmable metallization cell embodiment, and where "A" is Ge, at least one of materials 16 and 26 comprises silver. During formation of layer 26, some of it might diffuse into layer 23. Layer 26 and any remnant material 24 received directly over chalcogenide comprising material 23 will constitute one electrode of the resistance variable device being fabricated, with layer 16 constituting another or second electrode for the device.

Referring to Fig. 6, materials 24 and 26 are patterned into an electrode 30. Patterning to produce electrode 30 is typically and preferably conducted utilizing photolithography. Such provides but one preferred example of forming a second electrode material operatively proximate the chalcogenide comprising material. In a preferred embodiment, such results in the formation of a non-volatile resistance variable device which is fabricated into a programmable memory cell of memory circuitry. In one preferred embodiment, the device is finally formed to have a concentration of metal in chalcogenide comprising material 23 of less than 30% atomic in a lowest of a plurality of variable resistance states.

Referring to Fig. 7, one or more dielectric layers 32 are ultimately formed over the device. Of course, intervening conductive and semiconductive layers might also be provided to form other lines and devices outwardly of the depicted device.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.